JC14 Rec'd PCT/PTO 12 DEC 2001

FORM PTO-1390 (REV 11-2000)	U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 124-909
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known, see 37 C F R. 1 5) 10/009530 unknown
INTERNATIONAL APPLICATION NO. **PCT/GB00/02145**	INTERNATIONAL FILING DATE **02/06/2000**	PRIORITY DATE CLAIMED **14/06/1999**

TITLE OF INVENTION

METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

APPLICANT(S) FOR DO/EO/US

MARTIN, T et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The U.S. has been elected by the expiration of 19 months from the priority date (Article 31).
5. A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 34.
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has **NOT** expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 To 20 below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information. PTO Form 1449, Intl. Search Report and Cited References

584461

JC13 Rec'd PCT/PTO 12 DEC 2001

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) 10/009550 unknown	INTERNATIONAL APPLICATION NO. **PCT/GB00/02145**	ATTORNEY'S DOCKET NUMBER **124-909**

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5):

- -- Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1040.00
- -- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO....................$890.00
- -- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO $740.00
- -- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)..............................$710.00
- -- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4).......................................$100.00

						CALCULATIONS		PTO USE ONLY
ENTER APPROPRIATE BASIC FEE AMOUNT =						$	890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).						$	130.00	
CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE				
Total Claims	5	-20 =	0	X	$18.00	$	0.00	
Independent Claims	1	-3 =	0	X	$0.00		0.00	
MULTIPLE DEPENDENT CLAIMS(S) (if applicable)				$280.00		$	0.00	
CLAIM FEES ARE NOT BEING PAID AT THIS TIME			**TOTAL OF ABOVE CALCULATIONS =**			$	**1020.00**	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.							0.00	
SUBTOTAL =						$	**1020.00**	
Processing fee of $130.00, for furnishing the English Translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)). +							0.00	
TOTAL NATIONAL FEE =						$	**1020.00**	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). **$40.00** per property +						$	0.00	
Fee for Petition to Revive Unintentionally Abandoned Application ($1280.00 – Small Entity = $640.00)						$	0.00	
TOTAL FEES ENCLOSED =						$	**1020.00**	
						Amount to be: refunded	$	
						Charged	$	

a. ☒ A check in the amount of $1020.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 14-1140 in the amount of $_____ to cover the above fees. A duplicate copy of this form is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-1140. A duplicate copy of this form is enclosed.

d. ☒ The entire content of the foreign application(s), referred to in this application is/are hereby incorporated by reference in this application.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

NIXON & VANDERHYE P.C.
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SIGNATURE

Arthur R. Crawford
NAME

25,327 REGISTRATION NUMBER

December 12, 2001 Date

584461

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

MARTIN, T. et al. — Atty. Ref.: 124-909

Serial No. unknown — Group:

Filed: December 12, 2001 — Examiner:

For: METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

* * * * * * * * * * *

December 12, 2001

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

In order to place the above-identified application in better condition for examination, please amend the application as follows:

IN THE SPECIFICATION

Please substitute the following paragraphs in the specification for corresponding paragraphs previously presented. A copy of the amended specification paragraphs showing current revisions is attached.

Page 1, before the first line, insert as a separate paragraph:

This application is the U.S. national phase of international application PCT/GB00/02145 filed 02/06/2000, which designated the U.S..

IN THE CLAIMS

Please substitute the following amended claims for corresponding claims previously presented. A copy of the amended claims showing current revisions is attached.

3. A method according to Claim 1 characterised in that the mechanical shadow mask comprises a silicon wafer (92) having etched apertures (23) and an oxide film coating (91) upon which deposition does not occur at temperatures used for growth by chemical beam epitaxy.

4. A method according to claim 1 characterised in that the semiconductor device is a device (31, 100) for guiding radiation.

REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made**."

Respectfully submitted,

NIXON & VANDERHYE P.C.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Page 1, before the first line, insert as a separate paragraph:

This application is the U.S. national phase of international application PCT/GB00/02145 filed 02/06/2000, which designated the U.S..

IN THE CLAIMS

3. A method according to Claim 1 ~~or 2~~ characterised in that the mechanical shadow mask comprises a silicon wafer (92) having etched apertures (23) and an oxide film coating (91) upon which deposition does not occur at temperatures used for growth by chemical beam epitaxy.

4. A method according to ~~any preceding~~ claim 1 characterised in that the semiconductor device is a device (31, 100) for guiding radiation.

METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

The invention relates to a method of fabricating a semiconductor device with a tapered epitaxial layer.

Opto-electronic systems contain optical fibres and opto-electronic semiconductor devices such as lasers, amplifiers, modulators, detectors and switches. The size and shape of the optical modes supported by optical fibres are significantly different to those within opto-electronic semiconductor devices, and this results in modal mismatch and high optical losses when optical radiation is coupled between such devices and fibres.

One technology which reduces such optical losses involves the use of a microlens placed between the opto-electronic semiconductor device and the optical fibre. The microlens changes the size of the optical mode output by the opto-electronic semiconductor device or optical fibre, but not the shape of the mode. Another technology involves the use of an optical mode-converting waveguide placed between the opto-electronic semiconductor device and the optical fibre. Both of these technologies demand very high alignment tolerances with the result that the alignment of the components can represent the most significant part of the total cost of an opto-electronic system.

A third technology which reduces coupling losses involves the use of opto-electronic semiconductor devices having output waveguides with a two-dimensional tapered thickness profile between the active part of the device and the output facet. This tapering of the output waveguide allows the relatively small (0.5 to 2.0 μm) and sometimes highly asymmetric optical mode from the active part of an opto-electronic semiconductor device to be closely matched to the larger (6 to 10 μm), circularly symmetric optical mode supported by an optical fibre.

Lateral tapering of the output waveguide of an opto-electronic semiconductor device, i.e. tapering in a plane parallel to a substrate surface, may be achieved using known semiconductor processing techniques such as photolithography and chemical etching. This is carried out after epitaxial growth of the wafer from which the device is made.

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Tapering the core layer of a waveguide in a plane perpendicular to the plane of epitaxial layer on which it is grown is more difficult and involves controlling the thickness of the core layer during wafer growth.

Methods currently used for producing vertically tapered and flared semiconductor optical waveguides are described by Moerman in IEEE Journal of Selected Topics in Quantum Electronics, Volume 3 , Number 6, pp 1308 - 1320 and may be classified under three main headings, as follows:

Etching and re-growth techniques:
In these techniques, epitaxial growth of the wafer is stopped after deposition of the core layer of the waveguide. The wafer is then removed from the wafer growth apparatus and the core layer is etched to produce the required taper profile. The wafer is then replaced in the growth apparatus and the upper guiding layer is grown over the etched core layer. These techniques have the following disadvantages. First, the overall processing is complex and time-consuming. Second, removal of the partially-grown wafer from the growth apparatus and etching the waveguide core layer introduces contamination into the waveguide, increasing optical losses and reducing yield. Third, these methods have very low reproducibility. In one such method, known as dip-etching, it not possible to process the whole surface of a wafer.

Impurity-induced disordering:
This is a technique for producing vertically tapered waveguides starting with a waveguide in which the core layer has a uniform thickness. This technique is limited in that the initial uniform waveguide must have a core layer consisting of a multiple quantum-well region. Zinc is diffused into the waveguide through the upper guiding layer and penetrates the core layer to depth which varies with lateral position, i.e. position in the plane of the epitaxial layers. Where zinc has diffused, the refractive index of the core layer is reduced to that of the guiding layers, producing vertical tapering of the waveguide. This technique has low reproducibility, and the resulting waveguides have significant optical loss in the regions where zinc diffusion occurs. It is also limited in respect of the material systems that may be used.

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Epitaxial techniques:

Several techniques exist in which the tapered core layer and upper guiding layer of a waveguide may be grown in a single step. For example, a temperature gradient introduced in the plane of a wafer consisting of a substrate and a lower guiding layer during the growth of the core layer by molecular beam epitaxy (MBE) may be used to control the thickness of that layer. In this technique it is very difficult to control the compositional uniformity of ternary and quaternary compounds across the temperature gradient and materials having a low melting point or requiring a high growth temperature may have a narrow range of suitable growth temperatures. This places limits on the temperature gradients that may be employed.

Another epitaxial technique is known as "growth-on-a-ridge". By standard etching methods a ridge of varying width may be produced on a wafer comprising a substrate and a lower guiding layer. Due to surface diffusion properties of metal-organic vapour-phase epitaxy (MOVPE), the growth rate of the remaining waveguide layers increases as the width of the ridge decreases, producing a tapered waveguide. This technique involves complicated and time-consuming wafer processing before epitaxial growth of the core and upper guiding layers can take place.

Yet another epitaxial technique is shadow-mask MOVPE growth using a dielectric mask. In this technique, a patterned dielectric mask is deposited onto a wafer. During MOVPE epitaxial growth, deposition takes place through a window in the shadow mask. The lateral thickness of the layer deposited underneath the shadow mask may be controlled by varying the lateral dimensions of the window, the distance between the mask and the substrate, and the reactor pressure. This technique involves an additional growth step of growing the dielectric mask and an additional processing step to remove it. It also involves processing steps to pattern the mask which involve considerable delay and may leave the surface contaminated. Although a mechanical shadow mask may be used instead of a dielectric mask, MOVPE growth inevitably results in compositional non-uniformity within the tapered layer due to the unequal diffusion lengths of the reaction gases in MOVPE growth. This results in refractive index non-uniformity within the tapered layer which adversely affects the guiding of light within that layer. Also, exposure of the wafer to the atmosphere during mask insertion and removal may result in

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contamination of the wafer. A further disadvantage is that deposition of material on the mask itself necessitates mask cleaning or replacement.

US patent number 4 855 255 discloses a method for growing a tapered epitaxial layer by, *inter alia*, chemical beam epitaxy. The method involves the generation of thermal gradients across the surface of a substrate upon which the tapered layer is to be grown, in order to spatially control the rate at which epitaxial growth takes place at various positions on the substrate.

It is an object of the invention to provide an alternative process for fabricating a semiconductor optical slab-waveguide.

According to an aspect of the invention, there is provided method of fabricating a semiconductor device including a step of growing a tapered epitaxial layer upon a supporting surface in a single epitaxial growth step by chemical beam epitaxy, the plane of the taper being substantially perpendicular to the supporting surface, characterised in that the tapered epitaxial layer is grown using a mechanical shadow mask.

The invention makes it possible to fabricate a waveguide incorporating a core layer which tapers continuously in a plane perpendicular to the plane of a substrate on which the waveguide is fabricated. In tapered waveguides grown by MOVPE, the core layer thickness first increases before tapering to the thin part of the core. This adversely affects the guiding properties and optical loss of the waveguide and is avoided in the present process. Furthermore, compositional inhomogeneities present in tapered regions of waveguides produced by MOVPE growth are avoided due to the absence of gas phase reactions in CBE growth. The present method makes it possible to avoid uncontrolled changes in thickness and refractive index during epitaxial growth that may affect the guiding properties of a waveguide or increase its optical loss.

The tapered epitaxial layer may be grown in the same growth step as an untapered epitaxial layer. This allows wafer fabrication for devices having both tapered and untapered layers to be carried out without interruption of growth, which can lead to

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contamination and reduced device performance. Such wafer fabrication is relatively simple and rapid, allowing relatively inexpensive production on an industrial scale.

Preferably the mechanical shadow mask has an oxide coating upon which deposition does not occur at temperatures used for growth by chemical beam epitaxy. As there is no polycrystalline growth on the shadow mask during epitaxial growth, a shadow mask used in the method maintains its definition during epitaxial growth and may be re-used without cleaning in further growth runs. This is in contrast to growth by MBE where significant polycrystalline growth occurs on the shadow mask causing unwanted shadowing effects.

The method may be used to fabricate a semiconductor device for guiding radiation, for example an optical waveguide.

In order that the invention may be more fully understood, embodiments thereof will now be described, by way of example only, with reference to the accompanying drawings in which:

Figures 1 to 4 show the principal stages in a process according to the invention for producing a semiconductor optical waveguide with a core layer which is tapered in two dimensions,

Figure 5 shows a vertical section of a mechanical apparatus used during production of the waveguide,

Figure 6 shows a vertical section of a shadow mask used in the process,

Figure 7 shows a plan view of the shadow mask, and

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Figure 8 shows the structure of an opto-electronic semiconductor modulator which may also be produced by a process of the invention and which has a core layer which is tapered in two dimensions.

Referring to Figure 1, there is shown a portion of a vertical section through a gallium arsenide (GaAs) substrate wafer 10. The substrate 10 is prepared for epitaxial growth according to standard procedures familiar to those skilled in the art of semiconductor device fabrication. The substrate 10 is mounted in a molybdenum holder (not shown). The mounted substrate 10 is loaded into a chemical beam epitaxy (CBE) apparatus (not shown) and is then stored under ultra-high vacuum (UHV). It is then loaded into the growth chamber of the CBE apparatus under UHV conditions and heated to approximately 650 °C under an arsenic overpressure to remove oxide deposits on the surface whilst maintaining a stable surface and avoiding roughening. The temperature of the substrate 10 is then set to a growth temperature in the range 400 to 700 °C, typically 540 °C, to reduce unintentional incorporation of impurities during CBE growth using the preferred sources. Referring to Figure 2, the following layers are successively deposited by CBE uniformly over the surface of the substrate 10 in the following order:

a 0.5 μm layer 11 of GaAs,
a 3.5 μm layer 12 of AlGaAs having an aluminium mole fraction of 0.05 ± 0.005,
a 0.4 μm layer 13 of AlGaAs having an aluminium mole fraction of 0.3 ± 0.03, and
a 1.8 μm layer 14 of GaAs.

During CBE growth of the layers 11 to 14, the CBE reactor pressure is kept below 10^{-3} Torr so that gas phase reactions are avoided and the substrate 10 is rotated at 60 revolutions per minute. The layer 11 is a buffer layer which separates waveguide layers from the substrate 10. Layers 12 and 13 form lower guiding layers in the finished waveguide. The thickness of layer 14 is equal to that of a thin region of the tapered core layer in the finished waveguide. The substrate 10 and the layers 11 to 14 constitute a partially grown wafer 28. Following deposition of the layer 14 the arsine flux is switched off and the temperature of the wafer 28 is reduced to 200°C to avoid roughening of its upper surface.

Referring now to Figure 3, a silicon dioxide coated silicon shadow mask 22 (of which an end portion is shown) having a series of apertures such as 23 is mounted in intimate contact with a tantalum spacer 20 in a molydenum carrier (not shown). The shadow mask 22 and spacer 20 are loaded into the growth chamber of the CBE apparatus under UHV conditions and clamped into position. The spacer 20 separates the shadow mask 22 from the exposed surface of the layer 14 by a distance of 100 μm. The arsine flux is switched on and the temperature of the wafer 28 is returned to a growth temperature which is the original growth temperature (540 °C) corrected for an increase in surface temperature of the wafer 28 as a result of the shadow mask 22 reducing heat loss from it. CBE growth is then resumed. The environmental conditions in the CBE apparatus are such that CBE growth will take place on a chemically appropriate surface (i.e. layer 14) but not on an inappropriate surface (i.e. the surface of the mask 22). A 4 μm layer 16 of GaAs is grown over the layer 14 through the apertures in the shadow mask 22. In regions such as 29, close to the edges of the apertures in the mask 22, the growth rate is reduced so that the finished layer 16 has a thickness profile in the region 29 which tapers smoothly from zero to 4 μm over a lateral distance of approximately 1000 μm. Layers 14 and 16 form a homogeneous core layer 18 having tapered regions such as 15. It is believed that the profile of the tapers such as 15 is dominated by the angle at which chemical beams arrive at the wafer 28 during epitaxial growth. The length of the tapers 15 may be controlled by changing the thickness of the spacer 20 and the angle at which the chemical beams arrive at the wafer 28. This is in contrast to shadow mask growth by MOVPE where the taper profile is dominated by the geometry of apertures in the shadow mask and gas phase reactions so that the tapers' lengths may be limited by the diffusion length of molecules on the surface at a given temperature.

Growth of layer 16 is terminated by switching off the flux of group III -containing species to the growth chamber of the CBE apparatus. The temperature of the wafer 30 is reduced to 200 °C and the arsine supply to the CBE apparatus is switched off. The spacer 20 and shadow mask 22 are removed under UHV conditions. The arsine flux is then switched on and the temperature of the wafer 30 is returned to approximately 540 °C. CBE growth is then resumed. Referring now to Figure 4, a 1.2 μm thick layer 24 of AlGaAs having an aluminium mole fraction of 0.2 ± 0.02 is deposited on the upper surface of the layer 18 forming an upper guiding layer. A 0.1 μm capping layer 26 of GaAs is deposited uniformly over the upper guiding layer 24.

Epitaxial growth is then complete and the finished wafer 31 is removed from the CBE apparatus.

Lateral tapering of the waveguide, i.e. tapering in a plane parallel to the plane of the surface of the substrate 10, is then carried out by photolithography and reactive-ion etching in order to produce a laterally tapered ridge waveguide. Accurate photolithography may be achieved using a minimal length tapered alignment feature deposited through the shadow mask 22. The completed device is a passive ridge waveguide incorporating a core region which is tapered in two dimensions and which converts the size of an optical mode guided within it.

The CBE apparatus includes a stainless steel growth chamber having a rotatable heated substrate assembly, a gas inlet manifold, a stainless steel storage chamber for storage of substrates and shadow masks, a stainless steel loadlock chamber for loading and unloading substrates and shadow masks and a transfer mechanism for transferring substrates and shadow masks between chambers. The CBE apparatus also includes vacuum pumps to maintain UHV conditions within the chambers of the apparatus. During epitaxial growth, group III and group V chemical beams impinge on the surface of the substrate 10 at 45°.

Referring to Figure 5, there is shown a vertical section of a mechanical apparatus 50 which is used to hold the substrate 10, the spacer 20 and the shadow mask 22 within the CBE apparatus during epitaxial growth. The substrate 10 is mounted on a molybdenum carrier 52 and is secured in position by two tantalum springs 54. The substrate 10 has a major flat which sits firmly against a flat surface 56 of the carrier 52. The carrier 52 is attached to a heater assembly 58 by three pins such as 60. The spacer 20 and shadow mask 22 are mounted in a molybdenum holder 62 which is mounted onto the apparatus 50 over the substrate 10 by three pins such as 64, the spacer 20 being in contact with the substrate 10 around its edge. A clamping ring 66 having three springs 68 is mounted over the shadow mask 20 on the three pins to ensure contact between the spacer 20 and the substrate 10. The apparatus 50 gives minimum rotational error and accurate registration between the substrate 10 and shadow mask 22.

Referring now to Figure 6, there is shown a vertical section of the shadow mask 22. The mask 22 is fabricated from a silicon wafer having a thickness of 450 μm and a diameter of 75 mm. By standard procedures of photolithography and chemical etching, the <111> planes of the silicon wafer are etched to produce a series of apertures such as 23 with sloping sides such as 90 which are inclined at 54.7° to the plane of the silicon wafer. The remaining silicon 92 is coated with a thermal oxide film 91. Due to the chemical nature of CBE growth, there is no polycrystalline growth on the shadow mask 22 during epitaxial growth of layer 16. This is because decomposition of metal-containing alkyls does not occur on the oxide surface 91 of the mask 22 over a large temperature range in CBE growth. Figure 7 shows a plan view of the shadow mask 22 and also indicates the apertures 23 and the position of the substrate 10. The shadow mask 22 includes apertures 40 for the intrusion of the springs 54 and flat surface 56. The mask 22 also has holes 41 to enable it to be attached to the molybdenum carrier 62.

In a further embodiment of the invention, the process may be used to fabricate a tapered waveguide in which the guiding layers are of indium gallium arsenide phosphide (InGaAsP) and the tapered core layer is of indium phosphide (InP). Such a waveguide may be used for guiding and reshaping optical modes with wavelengths around 1.3 or 1.5 μm. In yet further embodiments of the invention, the process may be used to fabricate vertically tapered waveguides having core layers of indium arsenide (InAs), gallium antimonide (GaSb) or indium antimonide (InSb) for use with radiation having wavelengths between 1 and 8 μm.

The process of the invention may also be used to fabricate other semiconductor devices incorporating at least one tapered layer in a single epitaxial growth step. Figure 8 shows the structure of an opto-electronic semiconductor modulator 100 which may be fabricated by the process. The modulator 100 is fabricated as follows. An n-type GaAs substrate wafer 110 is prepared, mounted and loaded into a CBE apparatus as described above. The following epitaxial layers are then successively deposited on the wafer 110 by CBE in the following order:

a 0.5 μm layer 112 of n-type GaAs having a doping density of 10^{18} cm^{-3},

a 3.5 μm layer 114 of n-type AlGaAs having an aluminium mole fraction of 0.05 ± 0.005 and a doping density of 10^{18} cm^{-3},

a 0.3 μm layer 116 of n-type AlGaAs having an aluminium mole fraction of 0.3 ± 0.03 and a doping density of 10^{18} cm^{-3},

a 0.1 μm layer 118 of n-type AlGaAs having an aluminium mole fraction of 0.3 ± 0.03 and a doping density of 10^{17} cm^{-3},

a layer 120 of undoped GaAs having a tapered region 126 in which the thickness of the layer 120 increases from 1.8 μm to 5.8 μm over a lateral distance of approximately 1000 μm and which is formed using a spacer and shadow mask as described above,

a 1.2 μm layer 122 of undoped AlGaAs having an aluminium mole fraction of 0.2 ± 0.02, and

a 0.1 μm capping layer 124 of undoped GaAs.

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CLAIMS

1. A method of fabricating a semiconductor device including a step of growing a tapered epitaxial layer (18; 126) upon a supporting surface (13; 118) in a single epitaxial growth step by chemical beam epitaxy, the plane of the taper being substantially perpendicular to the supporting surface, characterised in that the tapered epitaxial layer is grown using a mechanical shadow mask (22).

2. A method according to Claim 2 characterised in that the tapered epitaxial layer is grown in the same growth step as an untapered epitaxial layer (12; 116).

3. A method according to Claim 1 or 2 characterised in that the mechanical shadow mask comprises a silicon wafer (92) having etched apertures (23) and an oxide film coating (91) upon which deposition does not occur at temperatures used for growth by chemical beam epitaxy.

4. A method according to any preceding claim characterised in that the semiconductor device is a device (31, 100) for guiding radiation.

5. A method according to Claim 4 characterised in that the semiconductor device is an optical waveguide (100).

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Fig.1.

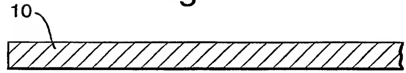


Fig.2.

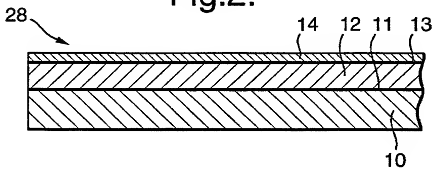


Fig.3.

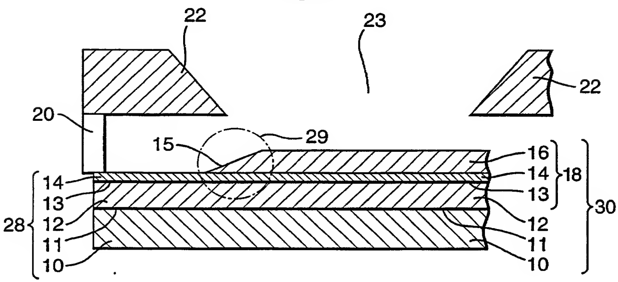
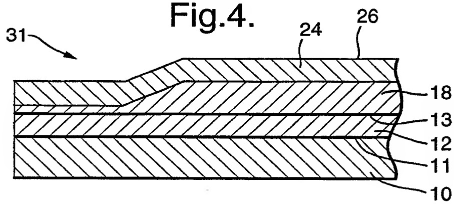


Fig.4.



10/009530

Fig.5.

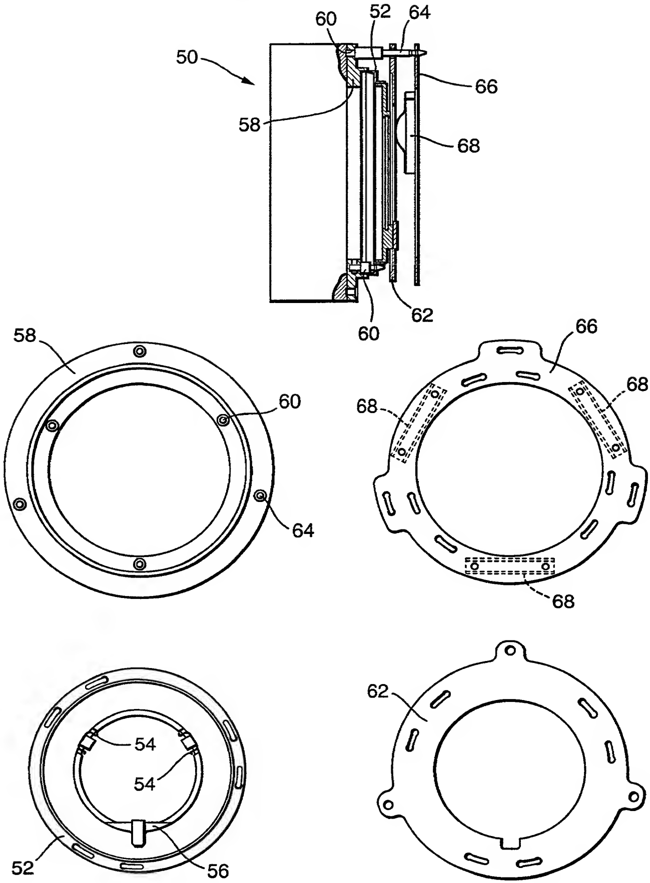
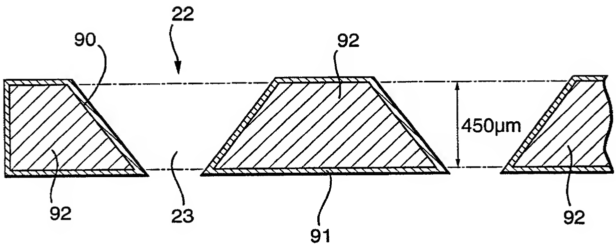


Fig.6.



10/009530

Fig.7.

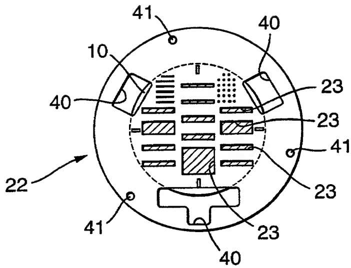
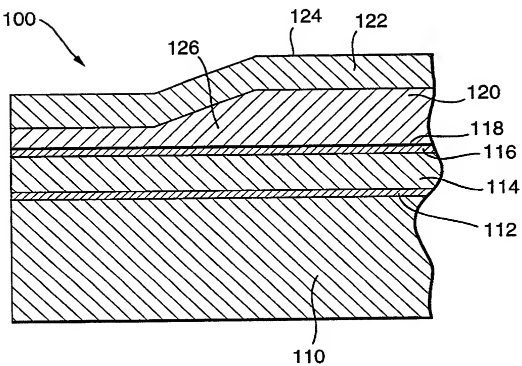


Fig.8.



RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

the specification of which (**check** applicable **box(s)**):

☐ is attached hereto

☐ was filed on ____ as U.S. Application Serial No. ____ Atty Dkt. No. P2844/1/USW

☒ was filed as PCT International application No. PCT/GB00/02145 on 02-Jun-2000

and (if applicable to U.S. or PCT application) was amended on 11-April-2001

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	**Country**	**Day/Month/Year Filed**
9913713.5	GB	14-Jun-1999

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	**Date/Month/Year Filed**

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

Prior U.S./PCT Application(s): Application Serial No.	**Day/Month/Year Filed**	**Status: patented pending, abandoned**
PCT/GB00/02145	02-Jun-2000	PENDING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. And I hereby appoint **NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 8th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed)**, and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S. Nixon, 25640; Robert A. Vanderhye, 27076; James T. Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E. Nusbaum, 32348; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Jeffry H. Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr. 29366; Thomas E. Byrne, 32205; Mary J. Wilson, 32955; J. Scott Davidson, 33489; Alan M. Kagen, 36178; William J. Griffin, 31260; Robert A. Molan, 29834; B. J. Sadoff, 36663; James D. Berquist, 34776; Updeep S. Gill, 37334; Michael J. Shea, 34725; Donald L. Jackson, 41090; Michelle N. Lester, 32331.*

DJb

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FOR ADDITIONAL INVENTORS, check box ☒ and attach sheet with same information and signature and date for each.

341317

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application Number	**Country**	**Day/Month/Year Filed**
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Prior U.S./PCT Application(s):

Application Serial No.	**Day/Month/Year Filed**	**Status: patented pending, abandoned**
PCT/GB00/02145	02-Jun-2000	.PENDING

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1. Inventor's Signature: T Martin Date: 22/11/01
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FOR ADDITIONAL INVENTORS, check box ☒ and attach sheet with same information and signature and date for each.

RULE 63 (37 C.F.R. 1.63)
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FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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5. Inventor's Signature: J.M. Heaton. Date: 23/11/01
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8. Inventor's Signature: Date:
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RULE 63 (37 C.F.R. 1.63)
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Nixon & Vanderhye P.C. (12/95)

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8. Inventor's Signature: Date:
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9. Inventor's Signature: Date:
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10. Inventor's Signature: Date:
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